What is claimed is:

1. A method of generating a pattern for a semiconductor device comprising:

a step of designing and arranging a layout pattern of a semiconductor chip;

a step of extracting an area ratio of the layout pattern; and

a step of adding and arranging a dummy pattern to the layout pattern, while consideration is given to the most appropriate area ratio of the layout pattern of the layer obtained according to a design rule of the layer composing the layout pattern, so that the area ratio of the layer can be the most appropriate area ratio.

2. A method of generating a pattern for a semiconductor device according to claim 1, further comprising:

a step of dividing the layout pattern formed in the layout pattern forming step into small regions of a desired size;

a step of extracting an area ratio of a mask pattern for each small region divided; and

a step of adding a dummy pattern so that the area ratio can be overlapped with the most appropriate area ratio of the mask pattern corresponding to the layout pattern,

wherein the area ratio of each small region is adjusted to be the same.

3. A method of generating a pattern for a semiconductor device according to claim 2, further comprising:

a step of preparing a plurality of types of dummy pattern cells, the area ratios of which are different from each other,

wherein the dummy pattern adding step include a step of selecting a desired dummy pattern cell from the dummy pattern cells according to the area ratio of the small region.

4. A method of generating a pattern for a semiconductor device according to claim 1,

wherein an area ratio after the completion of forming the dummy pattern is calculated, it is judged whether or not the area ratio is in a range of a predetermined condition, and when the area ratio is not in the range of the predetermined condition, several of the dummy patterns are replaced and the most appropriate dummy pattern cell is selected.

5. A method of generating a pattern for a semiconductor device according to claim 1, wherein the layout pattern forming step includes a step of forming a mask pattern for forming a wiring layer.

6. A method of generating a pattern for a semiconductor device according to claim 1, wherein the layout pattern forming step includes a step of forming a mask pattern for forming a diffusion layer.

7. A method of generating a pattern for a semiconductor device according to claim 1, wherein the layout pattern forming step includes a step of forming a mask pattern for forming a gate electrode.

8. A method of generating a pattern for a semiconductor device according to claim 1, wherein the layout pattern forming step includes a step of forming a mask pattern for forming a well.

9. A method of generating a pattern for a semiconductor device according to claim 1, further comprising a step of adjusting a layout in the vertical direction so that the dummy pattern cell can compose an MOS capacitor cell.

10. A method of generating a pattern for a semiconductor device according to claim 9, wherein the MOS capacitor cell is electrically connected to a power supply wiring and a ground wiring by a dummy pattern cell composed of an aggregation of the dummy patterns.

11. A method of generating a pattern for a semiconductor device according to claim 10, wherein the dummy pattern cell has a cross like pattern, and the dummy pattern cells on an upper and a lower layer of the cross like pattern mutually have an island-shaped isolated pattern corresponding to the cross region of the cross like pattern.

12. A method of generating a pattern for a semiconductor device according to claim 11, wherein the dummy pattern cell is composed of a first layer cell having a cross like pattern and an isolated island-shaped pattern in each of the four regions divided by the cross like pattern and also composed of a second layer cell, the pattern of which is a sharp-mark-shape arranged so that it crosses at four points corresponding to the four island-shaped pattern, located on an upper layer or a lower layer continuing to the first layer cell, and the first layer and the second layer respectively compose an electric power supply wiring and a ground wiring.

13. A device of generating a pattern used for a semiconductor device comprising:

a layout pattern forming means for forming a layout pattern from layout data of a semiconductor chip;

a space area detecting means for detecting a space area according to the layout pattern with respect to at least one layer of the layout pattern;

a most appropriate area ratio extracting means for extracting the most appropriate area ratio for forming the pattern of the layer according to a design rule; and

a dummy pattern arranging means for calculating an area ratio of the layer from the space area detecting means and arranging a dummy pattern so that the area ratio can be the most appropriate one.

14. A method of manufacturing a semiconductor device comprising:

a step of forming a mask pattern of each step according to a pattern for a semiconductor device generated by the method described in claim 1

and

a step of executing each process by using the mask pattern and forming a semiconductor device.

15. A semiconductor device comprising a pattern for a semiconductor device generated by the method described in claim 1.

16. A semiconductor device according to claim 15, wherein the pattern for a semiconductor device has an aggregation of dummy patterns of the same size not to be electrically connected, and at least one of the dummy patterns on each layer includes a region overlapped with a dummy pattern on an upper or a lower layer of the layer concerned in the vertical direction.

17. A method of manufacturing a semiconductor device comprising:

a step of forming a mask pattern of each step according to a pattern for a semiconductor device generated by the device described in claim 13;

and a step of executing each process by using the mask pattern and forming a semiconductor device.

18. A semiconductor device comprising a pattern for a semiconductor device generated by the device described in claim 13.